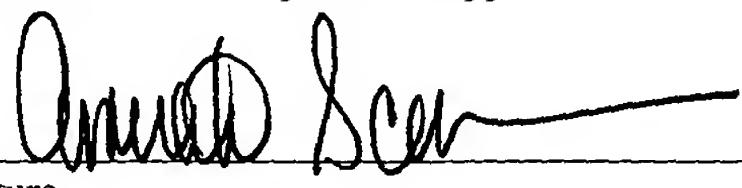
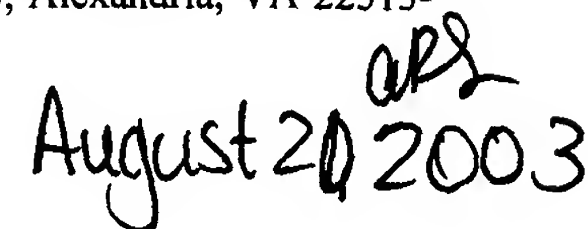


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**METHOD AND SYSTEM FOR ADJUSTING A FREQUENCY RANGE  
OF A DELAY CELL OF A VCO**

**FIELD OF THE INVENTION**

5           The present invention relates to voltage controlled oscillators (VCOs) and more particularly to VCO delay cells having an adjustable frequency range with essentially constant gain.

10           **BACKGROUND OF THE INVENTION**

          Voltage controlled oscillators (VCOs) are commonly employed in phase-locked loops (PLLs) that often provide clock recovery functionality in serial link communications. As its name implies, a VCO provides an oscillating signal with a frequency that depends on a control voltage. The frequency range of the VCO, i.e., the range of possible output frequencies for a particular range of input voltages, is an important aspect of a VCO. The ability to achieve a greater frequency range of a VCO allows greater opportunity to support more frequency ranges in a single serial link. While increasing the gain increases the frequency range, a problem exists with a corresponding increase in the noise/jitter component as the gain increases. Delay cells of a VCO typically do not cover a large

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frequency range while maintaining low VCO gain. Conventional methods of covering double the frequency range include the use of switchable dividers on output phases and the use of current starved cells that allow variation in tail current. Unfortunately, these methods also have their drawbacks, including increased complexity of the switchable dividers approach and increased random jitter problems with the tail current approach.

Accordingly, a need exists for a VCO delay cell with an adjustable frequency range that maintains substantially constant gain and avoids the problems of random jitter increase and increased complexity. The present invention addresses such a need.

## **SUMMARY OF THE INVENTION**

The present invention describes aspects of adjusting a frequency range of a delay cell of a VCO. The aspects include providing a CMOS latch of predetermined gain, and altering transconductance in the CMOS latch to alter a frequency range of the CMOS latch without altering the predetermined gain. The alteration of transconductance includes coupling at least one pair of series connected transistors in parallel with each switching device of the CMOS latch.

Through the present invention, minimization of random and deterministic jitter in a delay cell by maintaining low VCO gain is achieved while increasing the frequency range of the cell. Thus, the present invention provides a straightforward, effective, and efficient solution through enhancement of the features of a typical low noise cell to provide greater flexibility in selecting a frequency range achievable in the cell.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

Figure 1 illustrates a latch-type delay cell in accordance with the prior art.

Figure 2 illustrates a latch-type delay cell in accordance with the present invention.

Figure 3 illustrates a graph of frequency versus control voltage with data points from both HIGH and LOW control signal inputs for the circuit of Figure 2.

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## DESCRIPTION OF THE INVENTION

The present invention relates to adjusting a frequency range of a delay cell of a vco.

The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements.

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Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

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Figure 1 illustrates a latch-type delay cell 10 in accordance with the prior art for use in VCOs. The article, "A Low Noise, 900 MHz VCO in 0.6um CMOS" by Park and Kim, *IEEE Journal of Solid-State Circuits*, May 1999, details the operation of the cell 10. In general, the latch-type delay cell 10 of Figure 1 has a differential structure to reduce power-supply-injected phase noise and avoids the use of tail current source transistors. As described in the article and well-appreciated by those skilled in the art, the delay cell 10 includes a pair of cross-coupled NMOS transistors 12 and 14 that control a maximum gate voltage of PMOS load transistors 16 and 18 and limit the strength of the latch. Further coupled to NMOS transistors 12 and 14 and PMOS transistors 16 and 18 are NMOS transistors 20 and 22. In addition to transistors 12, 14, 16, 18, 20, and 22, which together basically form a simple differential inverter, the delay cell 10 includes PMOS transistors 24

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and 26 coupled in parallel with PMOS transistors 16 and 18 in order to handle negative skewed delay signals.

With the benefit of low noise achieved in the cell 10, the present invention expands on the cell of Figure 1 in order to allow greater adjustment to the frequency range of the cell while maintaining substantially constant gain. Figure 2 illustrates a circuit diagram of a delay cell 30 in accordance with a preferred embodiment of the present invention that alters the frequency range by achieving a higher power setting to choose a higher frequency range. The delay cell 30 includes a pair of series connected transistors in parallel with each of the switching devices of the delay cell 10, i.e., transistors 20, 22, 24, and 26. As shown, NMOS transistors 32 and 34 are coupled in series to each other and in parallel with NMOS transistor 20; NMOS transistors 36 and 38 are coupled in series to each other and in parallel with NMOS transistor 22; PMOS transistors 40 and 42 are coupled in series to each other and in parallel with PMOS transistor 24; and PMOS transistors 44 and 46 are coupled in series to each other and in parallel with PMOS transistor 26. As is further shown, the transistor of the series connected pair that is closest to the supply voltage (34, 38, 40, 44) has its gate connected to the switching node, which aids in maintaining the delay in the cell, while the cascode transistor of the pair (32, 36, 42, 46) has its gate connected to the control signal (HIGH or LOW).

With this arrangement, when a given pair of series connected transistors is enabled, the connections allow for the parallel path to be turned on for the corresponding switching device. This essential increase in the size of the switching device effectively increase the transconductance of the cell and causes the circuit to switch faster. In operation, when more frequency is desired, the parallel path is active in each of the legs of the circuit. However,

the control of the cell for the gain remains the same via the cross-coupled transistors in the cell. Thus, the frequency range of the cell is increased without increasing the gain and therefore without incurring increase in the jitter component. Of course, while a single pair of series connected transistors is shown in each leg, this is meant as illustrative and not restrictive of the number of pairs that may be included. Additional pairs may be included to further effectively increase the size of the cell and the frequency range, if desired, as is well appreciated by those skilled in the art.

Figure 3 illustrates a graph of frequency versus control voltage with data points from both HIGH and LOW control signal inputs for the circuit of Figure 2. The graph indicates an ability to achieve a shift in the frequency range without affecting the slope of the curve, i.e., the gain of the circuit. The lack of any increased gain maintains the low noise benefit of the cell.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.